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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,455	06/14/2006	Sylvain Duvillard	FR030154	6873

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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
10/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/596,455	DUVILLARD ET AL.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the main clock generator must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because of not commencing on a separate sheet. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Donnelly et al. (US 6,125,157) in view of Hiiragizawa (US 5,963,075).

With regard to claim 1, Donnelly et al. discloses in Fig. 22 a circuit comprising a plurality of interconnected logic blocks (3100, 3110, 3120); a main clock generator (3170) for distributing a reference clock signal (3140) to the logic blocks; at least one local clock generator in each logic block for generating a respective synchronized local clock signal from the reference clock signal for further provision to respective elements (3180, 3190) of the logic block. Fig. 22 of Donnelly et al. shows a circuit meeting all of the claimed limitations of claim 1, except that Donnelly et al. does not discloses the at least one local clock generator in each logic block generating a respective set of synchronized local clock signals as recited in the claim. The use of plural synchronized local clock signals, though not disclosed, nevertheless would have been obvious to a person having ordinary skill in the art because it is old and well-known in the art of circuit to use plural synchronized local clock signals (the motivation for this is to allow the circuit providing the plurality of synchronized local clock signals to the plurality of respective elements of the logic block). Furthermore, even thought Donnelly et al. does not discloses a set of local clock signals of a first block is phase shifted relative to a set of local clock signals of a second block. Hiiragizawa teaches in Figs. 5-9B a circuit having a local clock signal (111) of a

first block (104) is phase shifted relative to a local clock signal (112) of a second block (105) in order to inhibit all clock signals conduct the setting operation at the same time. Therefore, it would have been obvious to one of ordinary skill in the art to utilize that teaching of Hiiragizawa in the circuit of Donnelly et al. by having a set of local clock signals of a first block is phase shifted relative to a set of local clock signal of a second block for the advantage of being able to reduce the power consumption. Resultantly, the power consumption related to the setting operation can be minimized. Thus, claim 1 does not distinguish patentably over Donnelly et al. in view of Hiiragizawa.

With regard to claim 2, the first and second blocks communicate via a one-way data path (3150 in Fig. 22 of Donnelly et al.).

With regard to claims 3 and 4, the first block comprises a first logic cell configured to write data onto the one-way data path on a rising edge of one of the local clock signals of the first block provided at an enable input of the first logic cell and the second block comprises a second logic cell configured to read the written data from the one-way data path on a rising edge of one of the local clock signals of the second block provided at an enable input of the second logic cell /or on a failing edge of the reference clock signal provided at an enable input of the second logic cell (as depicted in Fig. 22 of Donnelly et al.). It would have been obvious to one of ordinary skill in the art to read/or write data on either a rising/or falling edge of the clock signal in order to meet the specific condition of the particular application.

With regard to claim 5, the circuit further comprises at least two additional blocks (3110, 3120) that communication via a two-way data bus (3150) and wherein respective sets of local clock signals of the at least two additional logic blocks are synchronized with each other.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Soderquist (US 5,982,238) is cited as of interest because it discloses a clock signal distribution and synchronization in a digital system.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HLN
October 4, 2007

N. DREW RICHARDS
SUPERVISORY PATENT EXAMINER